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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,623	01/28/2004	Chi-Hsing Hsu	JCLA8288-D	5651

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,623	HSU ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-13 and 18-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-13 and 18-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/144,121.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 6-13 and 18-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Cheng (U.S. Patent 6,353,999).

In re claim 6, **Cheng** discloses that a process for forming a semiconductor packaging substrate, comprising: forming a laminated circuit **216** having a first surface and a second surface opposite to the first surface, wherein the laminated circuit has a plurality of patterned internal metal layers **202b, 202c, 202d, and 202e** stacked up, and has a plurality of internal insulation layers **200** each of which is interposed between two adjacent internal metal layers **202b, 202c, 202d, and 202e**; forming at least one contact via **(unlabeled)** through the internal metal layers **202b, 202c, 202d, and 202e** and the internal insulation layers **200**, such that the internal metal layers **202b, 202c, 202d, and 202e** electrically connect to one another (col. 3, lines 39-55 and FIG. 6);

forming a first external insulation layer **214** (top) and a second external insulation layer **214** (bottom) respectively on the first surface and the second surface of the laminated circuit **216**, wherein the first external insulation layer **214** (top) has at least one first opening **210** and the external second insulation layer **214** (bottom) has at least one second opening **212**; forming a first via **218** (top) in the first opening **210** and a second

via **218** (bottom) in the second opening **212**; forming a first external metal layer **202a** on the first external insulation layer **214** (top) and a second external metal layer **202f** on the second external insulation layer **214** (bottom), wherein the first **202a** and second external metal layers **202f** are electrically connected to the internal metal layers **202b, 202c, 202d, and 202e** of the laminated circuit respectively through the first and second vias, and wherein the first external metal layer has a plurality of first externally exposed areas and the second external metal layer has a plurality of second externally exposed areas (col. 3, line 56 to col. 4, line 17 and FIG. 6).

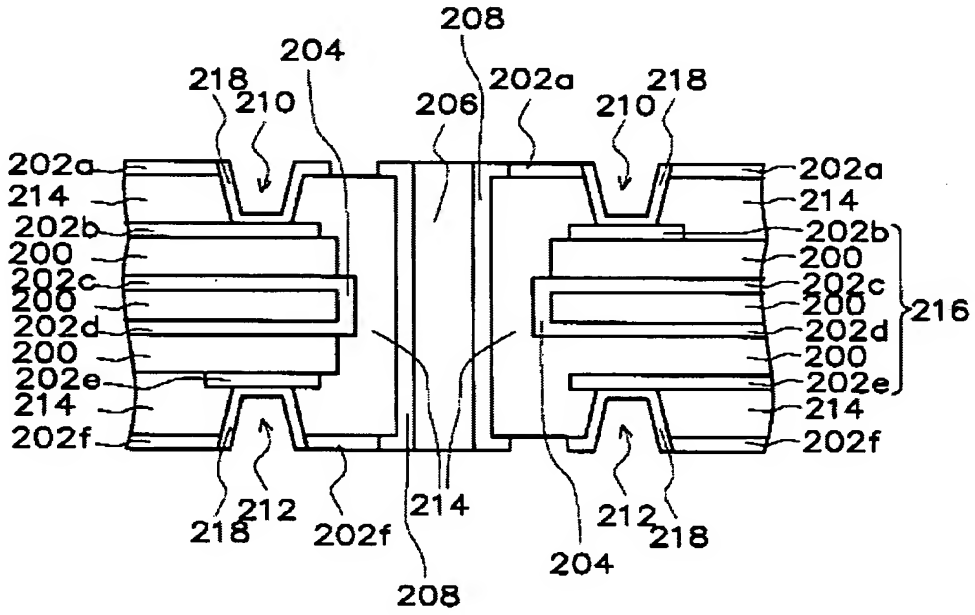

FIG. 6

In re claim 7, **Cheng** discloses that the forming the contact via **(unlabeled)** includes mechanically drilling and plating on the laminated circuit **216** (col. 3, lines 48-55).

In re claim 8, **Cheng** discloses that the forming the first **218** (top) and the second vias **218** (bottom) includes non-mechanically drilling an plating on the first **214** (top) and second **214** (bottom) external insulation layers, respectively (col. 3, line 63 to col. 4, line 17 and FIG. 6).

In re claim 9, **Cheng** discloses that the non-mechanically drill is selected from a group consisting of photo-via forming, laser ablating and plasma etching (col. 4, lines 3-17).

In re claim 10, **Cheng** discloses that the process of claim 6, further comprising a step of forming a first solder mask on the first external metal layer to cover the first external insulation layer and expose the first externally exposed areas, after forming the first external metal layer (FIG. 6).

In re claim 11, **Cheng** discloses that the process of claim 6, further comprising a step of forming a second solder mask on the second external metal layer to cover the second external insulation layer and expose the second externally exposed areas, after forming the second external metal layer (FIG. 6).

In re claim 12, **Cheng** discloses that the semiconductor packaging substrate is a flip-chip ball grid array packaging substrate (col. 4, lines 42-45).

In re claim 13, **Cheng** discloses that forming the internal metal layers **202b, 202c, 202d, and 202e** of the laminated circuit **216** includes forming and patterning copper foils (col. 3, lines 43-55).

In re claim 18, **Cheng** discloses a process for forming a semiconductor packaging substrate, comprising:

Performing a lamination process for forming a laminated circuit including the steps of: providing at least two sheets **200**, each sheet having a patterned conductive layer **202b, 202c, 202d, 202e** formed thereon; interposing a bonding sheet **200** between the two sheets; performing a thermal compression process so that the bonding sheet adheres the two sheets (col. 3, lines 39-55 and FIG. 6); and

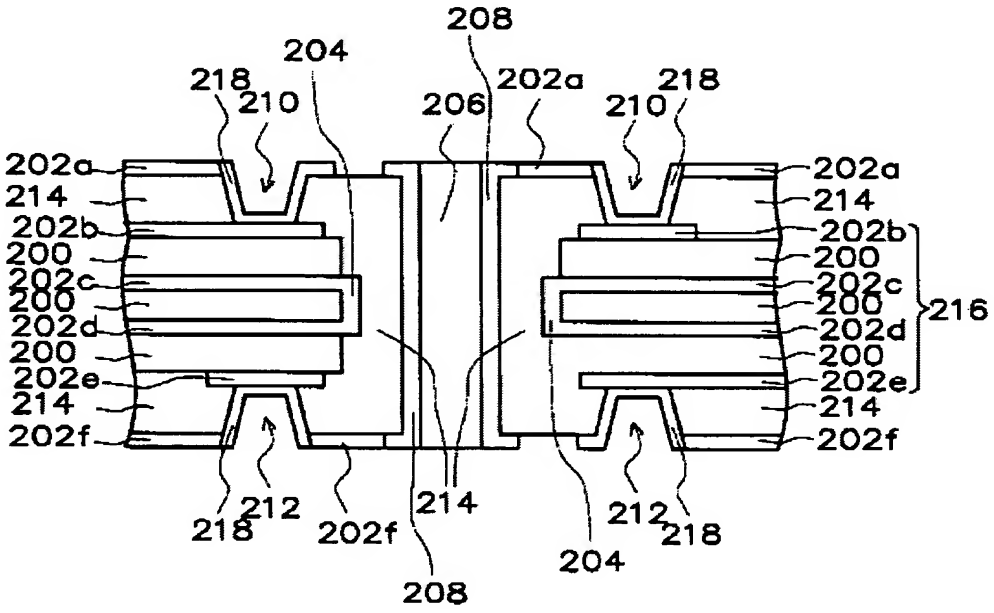

FIG. 6

forming at least one contact via (**unlabeled**) through the two sheets and the bonding sheet such that the patterned conductive layers formed on the two sheets are electrically connected to each other; and performing a build-up process comprising: forming a first insulation layer **214** (top) and a second insulating layer **214** (bottom) respectively on a first surface (top) and a second surface (bottom) of the laminated circuit **216**, wherein the first insulation layer comprises at least one first opening (unlabeled) and the second

insulation layer comprises at least one second opening (unlabeled); forming a first via in the first opening and a second via in the second opening; forming a first metal layer **202a** on the first insulation layer and a second metal layer **202f** on the second insulation layer, wherein the first metal layer **202a** and second metal layer **202f** are electrically connected to the patterned conductive layers of the laminated circuit respectively through the first and second vias **206** (col. 3, line 56 to col. 4, line 17 and FIG. 6).

In re claim 19, **Cheng** discloses that the step of forming the contact via includes mechanically drilling and plating process (col. 3, lines 48-55).

In re claim 20, **Cheng** discloses that the step of forming the first (top) and the second vias (bottom) includes non-mechanically drilling and plating process on the first **214** (top) and second **214** (bottom) external insulation layers, respectively (col. 3, line 63 to col. 4, line 17 and FIG. 6).

In re claim 21, **Cheng** discloses that the non-mechanically drilling is selected from a group consisting of photo-via forming, laser ablating and plasma etching (col. 4, lines 3-17).

In re claim 22, **Cheng** discloses that the process of claim 18, further comprising a step of forming a first solder mask on the first external metal layer to cover the first external insulation layer and expose the first externally exposed areas, after forming the first external metal layer (FIG. 6).

In re claim 23, **Cheng** discloses that the process of claim 18, further comprising a step of forming a second solder mask on the second external metal layer to cover the

second external insulation layer and expose the second externally exposed areas, after forming the second external metal layer (FIG. 6).

In re claim 24, **Cheng** discloses that the semiconductor packaging substrate is a flip-chip ball grid array packaging substrate (col. 4, lines 42-45).

In re claim 25, **Cheng** discloses that forming the internal metal layers **202b, 202c, 202d, and 202e** of the laminated circuit **216** includes forming and patterning copper foils (col. 3, lines 43-55).

Response to Applicants' Amendment and Arguments

Applicant's arguments filed October 4th, 2005 have been fully considered but they are not persuasive.

Applicants contend that the reference Cheng (U.S. Patent 6,353,999) herein known as Cheng fails to teach or disclose a semiconductor packaging substrate comprising at least a laminated circuit; and forming a first external insulation layer and a second external insulation layer respectively on the first surface and the second surface of the laminated circuit as required by the proposed independent claims.

In response to Applicants' contention that Cheng fails to teach or disclose a semiconductor packaging substrate comprising at least a laminated circuit; and forming a first external insulation layer and a second external insulation layer respectively on the first surface and the second surface of the laminated circuit as required by the proposed independent claims, Examiner respectively disagrees.

Applicants are directed to (col. 3, line 36 to col. 4, line 17 and FIG. 6) where Cheng clearly disclose a semiconductor packaging substrate comprising at least a

laminated circuit 216 obtained through the intermediate steps wherein a first external insulation layer 214 (top) and a second external insulation layer (bottom) are respectively formed on the first surface (top) and the second surface (bottom) of the laminated circuit 216. Thus, Cheng does teach Applicants' claimed invention.

For this reason, Examiner holds the rejection proper.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
December 18, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER